In the Claims:

1. (currently amended) Apparatus comprising:

a semiconductor body having on a surface thereof at least one lower antifuse and at least one upper antifuse in vertically stacked relation with both such antifuses sharing a common intermediate electrode therebetween;

the lower antifuse having a lower counter electrode and a lower fusible insulator portion defining a lower fuse element of an initial high electrical resistance state interconnecting the lower counter electrode with the common intermediate electrode; and

the upper antifuse having an upper counter electrode and an upper fusible insulator portion defining an upper fuse element of an initial high electrical resistance state interconnecting the upper counter electrode with the common intermediate electrode, wherein the upper antifuse is in the form of a contact antifuse defining a conductive contact interposed between the upper counter electrode and the upper fusible insulator portion defining the upper fuse element and interconnecting the upper counter electrode with the upper fuse element, the upper fuse element also being directly interconnected with the common intermediate electrode;

the upper and lower antifuses being arranged to permit their respective selective energizing for corresponding separate or simultaneous activation to a final low electrical resistance state.

Claims 2-5 (cancelled).

6. (original) The apparatus of claim 1 wherein the counter electrode of at least one of the antifuses is interconnected by the corresponding fuse element to the common intermediate electrode through at least one electrode extension portion interposed between said fuse element and the common intermediate electrode.

7. (original) The apparatus of claim 1 wherein the counter electrode of at least one of the antifuses is interconnected by the corresponding fuse element to the common intermediate electrode through at least one electrode extension portion interposed between said fuse element and the corresponding counter electrode.

8. (currently amended) Apparatus comprising:

a semiconductor body having on a surface thereof at least one lower antifuse and at least one upper antifuse in vertically stacked relation with both such antifuses sharing a common intermediate electrode there-between;

the lower antifuse having a lower counter electrode and a lower fusible insulator portion defining a lower fuse element of an initial high electrical resistance state interconnecting the lower counter electrode with the common intermediate electrode; and

the upper antifuse having an upper counter electrode and an upper fusible insulator portion defining an upper fuse element of an initial high electrical resistance state interconnecting the upper counter electrode with the common intermediate electrode;

the upper and lower antifuses being arranged to permit their respective selective energizing for corresponding separate or simultaneous activation to a final low electrical resistance state;

~~The apparatus of claim 1~~ wherein the lower antifuse is in the form of a gate oxide antifuse having a source region and a drain region correspondingly closely laterally adjacent the lower fusible insulator portion defining the lower fuse element, a gate oxide electrode in contact with the lower fuse element and forming the lower counter electrode, a source conductive extension portion interposed between the source region and the common intermediate electrode, the source conductive extension portion and source region together defining a source electrode extension portion, and a drain conductive extension portion interposed between the drain region and the common intermediate electrode, the drain conductive extension portion and drain region together defining a drain electrode extension portion, for interconnecting the gate oxide electrode by the lower fuse element with the common intermediate electrode through the source electrode extension portion and through the drain electrode extension portion.

9. (currently amended) The apparatus of claim 1 wherein the ~~upper antifuse is in the form of a~~ contact antifuse ~~having~~ further comprises an electrode extension portion ~~defining a conductive contact~~ interposed between the upper counter electrode and the upper fusible insulator portion ~~defining the upper fuse element and interconnecting the upper counter electrode with the upper fuse element, the upper fuse element also being interconnected with the common intermediate electrode~~.

Claims 10-15 (cancelled).

16. (currently amended) Apparatus comprising:

a semiconductor body having on a surface thereof at least one lower antifuse and at least one upper antifuse in vertically stacked relation with both such antifuses sharing a common intermediate electrode therebetween;

the lower antifuse having a lower counter electrode and a lower fusible insulator portion defining a lower fuse element of an initial high electrical resistance state interconnecting the lower counter electrode with the common intermediate electrode;

the upper antifuse having an upper counter electrode and an upper fusible insulator portion defining an upper fuse element of an initial high electrical resistance state interconnecting the upper counter electrode with the common intermediate electrode;

the upper and lower antifuses being arranged to permit their respective selective energizing for corresponding separate or simultaneous activation to a final low electrical resistance state; and

~~The apparatus of claim 1~~ further comprising energizable fuse activation circuit means defining a lower fuse activation circuit for applying and controlling a selective blow voltage across the lower counter electrode and common intermediate electrode at the lower fuse element for fusibly blowing the lower antifuse to a final low electrical resistance state to interconnect electrically conductively the lower counter electrode and the common intermediate electrode thereat, and further defining an upper fuse activation circuit for applying and controlling a selective blow voltage across the upper counter electrode and common intermediate electrode at the upper fuse element for fusibly blowing the upper antifuse to a final low electrical resistance state to interconnect electrically conductively the upper counter electrode and the common intermediate electrode thereat.

17. (original) The apparatus of claim 16 further comprising unblown or blown fuse activation state sensing and indicating circuit means defining a lower fuse state sensing and indicating circuit for sensing and indicating the unblown or blown fuse activation state of the lower antifuse, and further defining an upper fuse state sensing and indicating circuit for sensing and indicating the unblown or blown fuse activation state of the upper antifuse.

18. (original) The apparatus of claim 16 wherein the fuse activation circuit means are arranged for independently applying and controlling a selective blow voltage for fusibly blowing the lower antifuse, and for independently applying and controlling a selective blow voltage for fusibly blowing the upper antifuse, to permit their respective selective energizing for corresponding separate fuse activation.

19. (original) The apparatus of claim 16 wherein the fuse activation circuit means are arranged for simultaneously applying and controlling a selective blow voltage for fusibly blowing both the lower antifuse and upper antifuse, to permit their selective energizing for simultaneous fuse activation.

20. (original) The apparatus of claim 19 wherein the lower antifuse and upper antifuse are connected in parallel in the fuse activation circuit.

Claims 21-27 (cancelled).

28. (new) The apparatus of Claim 1, wherein the lower antifuse is in the form of a gate oxide antifuse having a source region and a drain region correspondingly closely laterally adjacent the lower fusible insulator portion defining the lower fuse element, a gate oxide electrode in contact with the lower fuse element and forming the lower counter electrode, a source conductive extension portion interposed between the source region and the common intermediate electrode, the source conductive extension portion and source region together defining a source electrode extension portion, and a drain conductive extension portion interposed between the drain region and the common intermediate electrode, the drain conductive extension portion and drain region together defining a drain electrode extension portion, for interconnecting the gate oxide electrode by the lower fuse element with the common intermediate electrode through the source electrode extension portion and through the drain electrode extension portion.

29. (new) The apparatus of Claim 8, wherein the upper antifuse is in the form of a contact antifuse defining a conductive contact interposed between the upper counter electrode and the upper fusible insulator portion defining the upper fuse element and interconnecting the upper counter electrode with the upper fuse element, the upper fuse element also being directly interconnected with the common intermediate electrode.

30. (new) The apparatus of Claim 16, wherein the upper antifuse is in the form of a contact antifuse defining a conductive contact interposed between the upper counter electrode and the upper fusible insulator portion defining the upper fuse element and interconnecting the

upper counter electrode with the upper fuse element, the upper fuse element also being directly interconnected with the common intermediate electrode.

31. (new) The apparatus of Claim 30, wherein the lower antifuse is in the form of a gate oxide antifuse having a source region and a drain region correspondingly closely laterally adjacent the lower fusible insulator portion defining the lower fuse element, a gate oxide electrode in contact with the lower fuse element and forming the lower counter electrode, a source conductive extension portion interposed between the source region and the common intermediate electrode, the source conductive extension portion and source region together defining a source electrode extension portion, and a drain conductive extension portion interposed between the drain region and the common intermediate electrode, the drain conductive extension portion and drain region together defining a drain electrode extension portion, for interconnecting the gate oxide electrode by the lower fuse element with the common intermediate electrode through the source electrode extension portion and through the drain electrode extension portion.

32. (new) The apparatus of Claim 16, wherein:

the upper antifuse is in the form of a contact antifuse defining a conductive contact interposed between the upper counter electrode and the upper fusible insulator portion defining the upper fuse element and interconnecting the upper counter electrode with the upper fuse element, the upper fuse element also being directly interconnected with the common intermediate electrode; and

the lower antifuse is in the form of a gate oxide antifuse having a source region and a drain region correspondingly closely laterally adjacent the lower fusible insulator portion defining the lower fuse element, a gate oxide electrode in contact with the lower fuse element and forming the lower counter electrode, a source conductive extension portion interposed between the source region and the common intermediate electrode, the source conductive extension portion and source region together defining a source electrode extension portion, and a drain conductive extension portion interposed between the drain region and the common intermediate electrode, the drain conductive extension portion and drain region together defining a drain electrode extension portion, for interconnecting the gate oxide electrode by the lower fuse element with the common intermediate electrode through the source electrode extension portion and through the drain electrode extension portion.

33. (new) An apparatus, comprising:

a semiconductor body having on a surface thereof at least one lower antifuse and at least one upper antifuse in vertically stacked relation, the upper and lower antifuse coupled to a common intermediate electrode formed between them;

the lower antifuse in the form of a gate oxide antifuse having a source region and a drain region formed on said surface, the drain region being coupled to said common intermediate electrode, the source region being coupled to a lower counter electrode, and a lower fuse element of a lower fusible insulator portion of initial high electrical resistance overlying said surface, a gate oxide electrode in contact with the lower fusible insulator portion for interconnecting the lower counter electrode and the common intermediate electrode;

the upper antifuse having an upper counter electrode and an upper fusible insulator portion of initial high electrical resistance defining an upper fuse element interconnecting the upper counter electrode with the common intermediate electrode; and

the upper and lower antifuses being arranged to permit their selective energizing for corresponding separate or simultaneous activation to a final low resistance electrical state.

34. (new) The apparatus of Claim 33, wherein the upper antifuse is directly connected to the common intermediate electrode.

35. (new) The apparatus of Claim 33, and further comprising upper and lower activation circuitry for selectively energizing the upper and lower antifuses separately or simultaneously.

36. (new) The apparatus of Claim 33 wherein the upper antifuse is in the form of a contact antifuse defining a conductive contact interposed between the upper counter electrode and the common intermediate electrode.

37. (new) An apparatus comprising:

a semiconductor body having a surface and overlying the surface in vertical relation:

an upper contact antifuse having an upper counter electrode and an upper fusible insulator portion defining an upper fuse element of initial high electrical resistance;

a common intermediate electrode in direct contact with the upper fusible insulator portion of said upper contact antifuse and opposing said upper counter electrode; and

a lower contact antifuse having a lower counter electrode and a lower fusible insulator portion defining a lower fuse element of initial high electrical resistance and interconnecting the lower counter electrode with the common intermediate electrode;

the upper and lower antifuses being arranged to permit their respective energizing for separate or simultaneous activation to a final low electrical state.

38. (new) The apparatus of Claim 37 wherein the lower contact antifuse is in the form of a gate oxide antifuse having a source region and a drain region formed on said surface, the drain region being coupled to said common intermediate electrode, the source region being coupled to a lower counter electrode, and a lower fuse element of a fusible insulator portion of initial high resistance overlying said surface and a gate oxide electrode in contact with the fusible insulator portion for interconnecting the lower counter electrode and the common intermediate electrode.

39. (new) The apparatus of Claim 37 and further comprising upper and lower activation circuitry for selectively energizing the upper and lower antifuses separately or simultaneously.

40. (new) The apparatus of Claim 37 wherein the upper antifuse is in the form of a direct contact antifuse defining a conductive contact interposed between the upper counter electrode and the upper fusible insulator portion defining the upper fuse element and interconnecting the upper counter electrode with the upper fuse element.

41. (new) An apparatus comprising:

a semiconductor body having a surface thereon and in vertically stacked relation:

at least one upper contact antifuse having an upper counter electrode and an upper fusible insulator portion defining an upper fuse element of initial high electrical resistance interconnected between the upper counter electrode and a common intermediate electrode; and

at least one lower contact antifuse having a lower counter electrode and a lower fusible insulator portion defining a lower fuse element of initial high electrical resistance and interconnecting the lower counter electrode with the common intermediate electrode;

an upper fuse activation circuit coupled for selectively energizing the upper fusible insulator portion to a final low resistance electrical state; and

a lower fuse activation circuit coupled for selectively energizing the lower fusible insulator portion to a final low resistance electrical state.

42. (new) The apparatus of Claim 41 wherein the upper and lower fuse activation circuits may energize the upper and lower fusible insulator portions separately.

43. (new) The apparatus of Claim 41 wherein the upper and lower fuse activation circuits may energize the upper and lower fusible insulator portions simultaneously.